

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

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1. (currently amended) An apparatus for controlling fixed-length cells of networking traffic in a networking hardware platform, the apparatus comprising at least one bi-directional first-in-first-out (FIFO) unit, wherein each bi-directional FIFO unit comprises a first unidirectional FIFO buffer and a second unidirectional FIFO buffer, the first and second unidirectional FIFO buffers each to buffer cells of which the cells of networking traffic are comprised, the cells that are buffered able to be delineated identified in the buffer through the use ~~in light~~ of a bits per word programmable parameter and a words per cell programmable parameter, the fixed length of the cells from which said cells of networking traffic is comprised being determinable from said bits per word parameter and said words per cell parameter.

2. (previously presented) The apparatus of claim 1, wherein the first and second unidirectional FIFO buffers each comprise asynchronous read and write ports.

3. (canceled)

4. (previously presented) The apparatus of claim 1 wherein the at least one bi-directional FIFO unit is: 1) configured to implement a write of at least one fixed-length cell sent from an interface; and is 2) configured to implement a read of at least one fixed-length cell destined to at least one asynchronous transfer mode (ATM) interface.

5. (previously presented) The apparatus of claim 1 wherein the first unidirectional FIFO buffer is configured to implement a write of at least one fixed-length cell sent from an ATM interface.

6. (previously presented) The apparatus of claim 1 wherein the first unidirectional FIFO buffer is configured to implement a write of at least one fixed-length cell sent from a frame relay interface.

7. (previously presented) The apparatus of claim 1 wherein the first unidirectional FIFO buffer is configured to implement a write of at least one fixed-length cell sent from a voice interface.

8. (previously presented) The apparatus of claim 1 wherein the first unidirectional FIFO buffer is configured to implement a write of at least one fixed-length cell sent from a data interface.

9. (previously presented) The apparatus of claim 1 wherein the first unidirectional FIFO buffer is configured to implement a read of at least one fixed-length cell destined to at least one switch, wherein the at least one switch handles fixed-length cells from sources having a plurality of bandwidths.

10. (previously presented) The apparatus of claim 9 wherein the at least one switch can route the at least one fixed-length cell to at least one service module.

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11. (previously presented) The apparatus of claim 10 wherein the at least one service module can provide the at least one fixed-length cell to a service subscriber using a T1, E1, T3, E3, OC3, or OC 12 port.

12. (previously presented) The apparatus of claim 1 wherein the second unidirectional FIFO buffer is configured to implement a read of at least one fixed-length cell destined to an ATM interface.

13. (previously presented) The apparatus of claim 1 wherein the second unidirectional FIFO buffer is configured to implement a read of at least one fixed-length cell destined to a frame relay interface.

14. (previously presented) The apparatus of claim 1 wherein the second unidirectional FIFO buffer is configured to implement a read of at least one fixed-length cell destined to a voice interface.

15. (previously presented) The apparatus of claim 1 wherein the second unidirectional FIFO buffer is configured to implement a read of at least one fixed-length cell destined to a data interface.

16. (previously presented) The apparatus of claim 1 wherein the second unidirectional FIFO buffer is configured to implement a write of at least one fixed-length cell sent from at least one switch wherein the at least one switch handles fixed-length cells from sources having a plurality of bandwidths.

17. (previously presented) The apparatus of claim 16 wherein the at least one switch can route the at least one fixed-length cell from a service module.

18. (previously presented) The apparatus of claim 17 wherein the service module can receive the at least one fixed-length cell from a service subscriber using a T1, E1, T3, E3, OC3, or OC 12 port.

19. (previously presented) The apparatus of claim 1 wherein the at least one bi-directional FIFO unit comprises a diagnostic interface, wherein the diagnostic interface supports a non destructive read of the at least one bi-directional FIFO unit while at least one fixed-length cell is being written to an read from the at least one bi-directional FIFO unit.

20. (previously presented) The apparatus of claim 1 wherein the at least one fixed-length cell is written to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer over a first enabled diagnostic loop.

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21. (previously presented) The apparatus of claim 1 wherein the at least one fixed-length cell is written to the first unidirectional FIFO buffer from the second unidirectional FIFO buffer over a second enabled diagnostic loop.

22. (previously presented) The apparatus of claim 1 wherein each unidirectional FIFO buffer outputs a write port fixed-length cell count, wherein a write port of each unidirectional FIFO buffer outputs a status indicating space available in the unidirectional FIFO buffer for at least one more fixed-length cell.

23. (previously presented) The apparatus of claim 22 wherein at least one master bi-directional FIFO unit is designed to cease writing at least one fixed-length cell to the first unidirectional FIFO buffer of at least one slave bi-directional

FIFO unit in response to the write port fixed-length cell count of the first unidirectional FIFO buffer, wherein the at least one master bi-directional FIFO unit disables at least one switch from routing at least one fixed-length cell to the at least one slave bi-directional FIFO unit in response to the write port fixed-length cell count, and wherein at least one switch routes the at least one fixed-length cell to another of the at least one slave bi-directional FIFO units in response to the write port fixed-length cell count of the first unidirectional FIFO buffer.

24. (previously presented) The apparatus of claim 23 wherein the at least one master bi-directional FIFO unit resumes writing the at least one fixed-length cell to the second unidirectional FIFO buffer of the at least one slaved bi-directional FIFO unit in response to the write port fixed-length cell count of the second unidirectional FIFO buffer, wherein the at least one master bi-directional FIFO unit enables at least one switch to route at least one fixed-length cell to the at least one slave bi-directional FIFO unit in response to the write port fixed-length cell count of the second unidirectional FIFO buffer.

25. (previously presented) The apparatus of claim 1 wherein each unidirectional FIFO buffer outputs a read port fixed-length cell count, wherein a read port of each unidirectional FIFO buffer outputs a status indicating space available in the unidirectional FIFO buffer for at least one cell.

26. (previously presented) The apparatus of claim 1 wherein write port logic of each unidirectional FIFO buffer is synchronous with a write clock.

27. (previously presented) The apparatus of claim 26 wherein the write clock operates at a frequency substantially equal to 50 megahertz.

28. (previously presented) The apparatus of claim 1 wherein read port logic of each unidirectional FIFO buffer is synchronous with a read clock.

29. (previously presented) The apparatus of claim 28 wherein the read clock operates at frequency substantially equal to 21 megahertz.

30. (previously presented) The apparatus of claim 28 wherein the read clock operates at a frequency substantially equal to 42 megahertz.

31. (previously presented) The apparatus of claim 1 wherein at least one invalid fixed-length cell can be discarded from each unidirectional FIFO buffer.

32. (previously presented) The apparatus of claim 1 wherein the switch platform further comprises two switches.

33. (previously presented) The apparatus of claim 1 wherein the networking hardware platform comprises at least one service module and at least one fixed-length cell bus controller, wherein the at least one fixed-length cell bus controller is coupled between the at least one service module and a least one switch, wherein the at least one service module comprises at least one slave bi-directional FIFO unit, and wherein the at least one fixed-length cell bus controller comprises at least one master bi-directional FIFO unit.

34. (currently amended) A networking hardware platform comprising:

- at least one service module;
- at least one fixed length cell bus controller coupled between the at least one service module and at least one switch;
- at least one bi-directional first-in-first-out (FIFO) unit located in the at least one fixed-length cell bus controller, wherein each bi-directional FIFO unit comprises a first and a second unidirectional FIFO buffer each capable of discarding an invalid fixed length cell, the first and second unidirectional FIFO buffers to buffer cells, the cells that are buffered able to be delineated identified in the buffer through the use ~~in light~~ of a bits per word programmable parameter and a words per cell programmable parameter, the fixed length of the cells being

determinable from the bits per word parameter and the words per cell parameter;
and

at least one diagnostic interface, wherein the at least one diagnostic interface supports a non-destructive read of the at least one bi-directional FIFO unit.

35. (previously presented) The network hardware platform of claim 34 wherein the at least one bi-directional FIFO unit is configured to write at least one fixed-length cell sent from an interface and read at least one fixed-length cell to be sent to the interface, wherein the interface is an asynchronous transfer mode (ATM) interface, a frame relay interface, a voice interface or a data interface.

36. (previously presented) The network hardware platform of claim 34 wherein at least one fixed-length cell can be written to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer over a first enabled diagnostic loop, and wherein at least one fixed-length transmission unit can be written to the first unidirectional FIFO buffer from the second unidirectional FIFO buffer over a second enabled diagnostic loop.

37. (previously presented) The network hardware platform of claim 34 wherein each unidirectional FIFO buffer outputs a write port fixed-length

cell count, wherein a write port of each unidirectional FIFO buffer outputs a status indication of space available in the unidirectional FIFO buffer for at least one more fixed-length cell.

38. (previously presented) The network hardware platform of claim 34 wherein the first and second unidirectional FIFO buffers each comprise asynchronous read and write ports, wherein the write port logic of each unidirectional FIFO buffer is synchronous with a write clock, and wherein the read port logic of each unidirectional FIFO buffer is synchronous with a read clock.

39. (canceled)

40. (previously presented) The network hardware platform of claim 34 wherein the at least one bi-directional FIFO unit is configured to read at least one fixed-length cell to be sent to the at least one switch and write at least one fixed-length transmission unit that has been sent from the at least one switch, wherein the switch handles fixed-length cells from sources having a plurality of bandwidths.

41. (previously presented) The network hardware platform of claim 34 wherein the at least one service module can receive at least one fixed-length cell

from and provide at least one fixed-length cell to at least one service subscriber using any one of a TI, EI, T3, E3, OC3, or OC 12 port.

42. (currently amended) A method for controlling fixed-length cells of networking traffic in a networking hardware platform, the method comprising transferring at least one fixed-length cell into a bi-directional first-in-first-out (FIFO) unit, wherein the bi-directional FIFO unit comprises a first unidirectional FIFO buffer and second unidirectional FIFO buffer, one of the unidirectional FIFOs to buffer egress cells, another of the unidirectional FIFOs to buffer ingress cells, the transferring further comprising reading or writing a cell from or to the first unidirectional FIFO, the cell read from or written to the first unidirectional buffer able to be delineated identified from other cells that are buffered within the first unidirectional buffer based upon of a bits per word programmable parameter and a words per cell programmable parameter, the fixed-length of the cells that the networking traffic is comprised of being determinable from the bits per word parameter and the words per cell parameter.

43. (previously presented) The method of claim 42 further comprising programming the word size of each of the first and second unidirectional FIFO buffers.

44. (previously presented) The method of claim 43 wherein the transferring further comprises:

synchronously writing the fixed-length cell from at least one port to the first unidirectional FIFO buffer; and

synchronously reading the fixed-length cell from the first unidirectional FIFO buffer and sending the fixed-length cell to switch, the reading being asynchronous with respect to the writing.

45. (previously presented) The method of claim 42 wherein the transferring further comprises:

synchronously writing the fixed-length cell en route from a switch to the first unidirectional FIFO buffer; and

synchronously reading the fixed-length cell from the first unidirectional FIFO buffer and sending it to at least one port, wherein the reading is asynchronous with respect to the writing.

46. (previously presented) The method of claim 42 further comprising:

discarding at least one invalid fixed-length cell from each unidirectional FIFO buffer; and

executing a non-destructive read of the at least one bi-directional FIFO unit while at least one fixed-length cell is being written to and read from the at least one bi-directional FIFO.

47. (previously presented) The method of claim 42 further comprising:

writing at least one fixed-length cell to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer using a first enabled diagnostic loop.

48. (previously presented) The method of claim 42 further comprising:

outputting a write port fixed-length cell count from each unidirectional FIFO buffer;

outputting a read port fixed-length cell count from each unidirectional FIFO buffer; and

outputting from a read port of each unidirectional FIFO buffer a status indicating space available in the unidirectional FIFO buffer for at least one more fixed-length cell.

49. (previously presented) The method of claim 42 wherein the plurality of ports comprise at least one asynchronous transfer mode (ATM) interface, at least one frame relay interface, at least one voice interface, at least one data interface, at least one network switch interface, at least one OC12 interface, or at least one OC3 interface.

50. (currently amended) An apparatus, comprising:

a bus master that controls:

1) a first bus that transports information from said bus master to one or more service modules that are coupled to said first bus;

2) a second bus that transports information from said one or more service modules to said bus master, said one or more service modules also coupled to said second bus, each of said service modules providing a networking interface,

said bus master further comprising:

a) a transmission output to said first bus that transmits egress information in fixed size portions to any of said service modules;

b) a reception input from said second bus that receives ingress information in fixed size portions from any of said service modules;

c) an egress first-in-first-out (FIFO) buffer that queues words from which said fixed size portions of egress information are comprised, said egress FIFO buffer further comprising:

1) an output from which said fixed size portions of egress information flow to said transmission output;

2) an input at which said fixed size portions of egress information are received, each of said fixed size portions of egress information including, when received at said input, a label that identifies which of said service modules a particular fixed size portion of egress information is to be sent to;

said fixed sized portions of queued egress information having boundaries made determinable ~~in light~~ through the use of a programmable bits per word size parameter for said egress FIFO buffer and a programmable words per fixed portion of egress traffic parameter, said fixed size of said portions of egress information being determinable from said egress FIFO bits per word size and said words per fixed portion of egress traffic parameters; and,

d) an ingress first-in-first-out (FIFO) buffer that queues words from which said fixed size portions of ingress information are comprised, said ingress FIFO buffer further comprising:

- 1) an output from which said fixed size portions of ingress information flow;
- 2) an input to which said fixed size portions of ingress information flow from said reception input, each of said fixed size portions of ingress information including, when received at said reception input, a label that

identifies which of said service modules a particular
fixed size portion of ingress information is being sent
from;

said fixed sized portions of queued ingress information having
boundaries made determinable ~~in light of~~ through the use of
programmable bits per word size parameter for said ingress
FIFO buffer and a programmable words per fixed portion of
ingress traffic parameter, said fixed size of said portions of
egress information being determinable from said ingress
FIFO bits per word size and said words per fixed size portion
of ingress traffic parameters.

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51. (previously presented) The apparatus of claim 50 wherein one of
said service modules can be used to provide Frame Relay service.

52. (previously presented) The apparatus of claim 51 wherein said
one of said service modules has a T1 networking interface.

53. (previously presented) The apparatus of claim 50 wherein one of
said service modules can be used to provide ATM service.

54. (previously presented) The apparatus of claim 53 wherein said
one of said service modules has a T1 networking interface.

55. (previously presented) The apparatus of claim 50 wherein said fixed size of said portions of egress information is the same as said fixed size of said portions of ingress information.

56. (previously presented) The apparatus of claim 55 wherein said fixed size can further comprise 56 bytes.

57. (previously presented) The apparatus of claim 50 further comprising a first counter that counts the number of words that have been stored into said egress FIFO buffer at said egress FIFO buffer input.

58. (previously presented) The apparatus of claim 57 further comprising a first reset value to which said first counter is set if said first counter reaches said words per fixed portion of egress traffic parameter.

59. (previously presented) The apparatus of claim 57 further comprising a second counter that counts the number of words that have been removed from said egress FIFO buffer at said egress FIFO buffer output.

60. (previously presented) The apparatus of claim 59 further comprising a second reset value to which said second counter is set if said

second counter reaches said words per fixed portion of egress traffic parameter.

61. (previously presented) The apparatus of claim 59 further comprising a third counter and a fourth counter that each:

1) increment in value if said first counter reaches said words per fixed portion of egress traffic parameter; and

2) decrement in value if said second counter reaches said words per fixed portion of egress traffic parameter.

62. (previously presented) The apparatus of claim 61 wherein said third counter is within the domain of a first clock that times the removal of words from said egress FIFO buffer and wherein said fourth counter is within the domain of a second clock that times the storing of words into said egress FIFO buffer.

63. (previously presented) The apparatus of claim 50 further comprising a first counter that counts the number of words that have been stored into said ingress FIFO buffer at said ingress FIFO buffer input.

64. (previously presented) The apparatus of claim 63 further comprising a first reset value to which said first counter is set if said first counter reaches said words per fixed portion of ingress traffic parameter.

65. (previously presented) The apparatus of claim 63 further comprising a second counter that counts the number of words that have been removed from said ingress FIFO buffer at said ingress FIFO buffer output.

66. (previously presented) The apparatus of claim 65 further comprising a second reset value to which said second counter is set if said second counter reaches said words per fixed portion of ingress traffic parameter.

67. (previously presented) The apparatus of claim 65 further comprising a third counter and a fourth counter that each:

1) increment in value if said first counter reaches said words per fixed portion of ingress traffic parameter; and

2) decrement in value if said second counter reaches said words per fixed portion of ingress traffic parameter.

68. (previously presented) The apparatus of claim 67 wherein said third counter is within the domain of a first clock that times the storing of words into said ingress FIFO buffer and wherein said fourth counter is within the domain of a second clock that times the removal of words from said ingress FIFO buffer.

69. (previously presented) A method, comprising:

programming a bits per word size parameter for an egress first-in-first-out (FIFO) buffer and programming a words per fixed portion of egress traffic parameter for said egress FIFO buffer;

programming a bits per word size parameter for an ingress first-in-first-out (FIFO) buffer and programming a words per fixed portion of ingress traffic parameter for said ingress FIFO buffer;

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sending fixed size portions of egress traffic from said egress FIFO buffer over a first bus to any of a plurality of service modules that are coupled to said first bus, each of said fixed size portions of egress traffic further comprising a label that identifies which service module a particular fixed size portion of egress traffic is sent to;

identifying a boundary of a fixed size portion of egress traffic within said egress FIFO buffer based upon said programmed bits per word size parameter for said egress FIFO and said programmed words per fixed portion of egress traffic parameter; and

sending fixed size portions of ingress traffic from any of said plurality of service modules over a second bus to said ingress FIFO buffer, [[,]] each of said fixed size portions of ingress traffic further comprising a label that identifies from which service module a particular fixed size portion of ingress traffic was sent;

identifying a boundary of a fixed size portion of ingress traffic within said ingress FIFO buffer based upon said programmed bits per word size

parameter for said ingress FIFO and said programmed words per fixed size portion of ingress traffic parameter.

70. (previously presented) The method of claim 69 wherein said fixed size of said portions of egress traffic is the same as said fixed size of said portions of ingress traffic.

71. (previously presented) The method of claim 70 wherein said fixed size can comprise 56 bytes.

72. (previously presented) The method of claim 69 further comprising counting, with a first count value, the number of words that have been stored into said egress FIFO buffer.

73. (previously presented) The method of claim 72 further comprising resetting said first count value to a first reset value if said first count value reaches said words per fixed portion of egress traffic parameter.

74. (previously presented) The method of claim 72 further comprising counting, with a second count value, the number of words that have been removed from said egress FIFO buffer.

75. (previously presented) The method of claim 74 further comprising resetting said second count value to a second reset value if said second count value reaches said words per fixed portion of egress traffic parameter.

76. (previously presented) The method of claim 74 further comprising counting with a third count value and counting with a fourth count value, said counting with a third and fourth count values further comprising:

1) incrementing said third and fourth count values if said first count value reaches said words per fixed portion of egress traffic parameter; and

2) decrementing said third and fourth count values if said second count value reaches said words per fixed portion of egress traffic parameter.

77. (previously presented) The method of claim 76 wherein said counting with a third count value is timed with a first clock that times the removal of words from said egress FIFO buffer and wherein said counting with a fourth count value is timed with a second clock that times the storing of words into said egress FIFO buffer.

78. (previously presented) The method of claim 69 further comprising counting, with a first count value, the number of words that have been stored into said ingress FIFO buffer.

79. (previously presented) The method of claim 78 further comprising resetting said first count value to a first reset value if said first count value reaches said words per fixed portion of ingress traffic parameter.

80. (previously presented) The method of claim 78 further comprising counting, with a second count value, the number of words that have been removed from said ingress FIFO buffer.

81. (previously presented) The method of claim 80 further comprising resetting said second count value to a second reset value if said second count value reaches said words per fixed portion of ingress traffic parameter.

82. (previously presented) The method of claim 80 further comprising counting with a third count value and counting with a fourth count value, said counting with a third and fourth count values further comprising:

1) incrementing said third and fourth count values if said first count value reaches said words per fixed portion of ingress traffic parameter; and

2) decrementing said third and fourth count values if said second count values reaches said words per fixed portion of ingress traffic parameter.

83. (previously presented) The method of claim 82 wherein said counting with a third count value is timed with a first clock that times the storing of words into said ingress FIFO buffer and wherein said counting with a fourth count value is timed with a second clock that times the removal of words from said ingress FIFO buffer.

84. (previously presented) An apparatus, comprising:

means for programming a bits per word size parameter for an egress first-in-first-out (FIFO) buffer and programming a words per fixed portion of egress traffic parameter for said egress FIFO buffer;
means for programming a bits per word size parameter for an ingress first-in-first-out (FIFO) buffer and programming a words per fixed portion of ingress traffic parameter for said ingress FIFO buffer;

means for sending fixed size portions of egress traffic from said egress FIFO buffer over a first bus to any of a plurality of service modules that are coupled to said first bus said fixed size portions of egress traffic further comprising a label that identifies which service module a particular fixed size portion of egress traffic is sent to;

means for identifying said fixed size portions of egress traffic within said egress FIFO buffer based upon said programmed bits per word size parameter for said egress FIFO and said programmed words per fixed size portion of egress traffic parameter; and,

means for sending fixed size portions of ingress traffic from any of said plurality of service modules over a second bus to said ingress FIFO buffer, each of said fixed size portions of ingress traffic further comprising a label that identifies from which service module a particular fixed size portion of ingress traffic was sent;

means for identifying said fixed size portions of ingress traffic within said ingress FIFO buffer based upon said programmed bits per word size parameter for said ingress FIFO and said programmed words per fixed size portion of egress traffic parameter.

85. (previously presented) The apparatus of claim 84 wherein said fixed size of said portions of egress traffic is the same as said fixed size of said portions of ingress traffic.

86. (previously presented) The apparatus of claim 85 wherein said fixed size can comprise 56 bytes.

87. (previously presented) The apparatus of claim 84 further comprising means for counting, with a first count value, the number of words that have been stored into said egress FIFO buffer.

88. (previously presented) The apparatus of claim 87 further comprising means for resetting said first count value to a first reset value if

said first count value reaches said words per fixed size portion of egress traffic parameter.

89. (previously presented) The apparatus of claim 87 further comprising means for counting, with a second count value, the number of words that have been removed from said egress FIFO buffer.

90. (previously presented) The apparatus of claim 89 further comprising means for resetting said second count value to a second reset value if said second count value reaches said words per fixed size portion of egress traffic parameter.

91. (previously presented) The apparatus of claim 89 further comprising means for counting with a third count value and counting with a fourth count value, said means for counting with a third and fourth count values further comprising:

1) means for incrementing said third and fourth count values if said first count value reaches said words per fixed size portion of egress traffic parameter; and

2) means for decrementing said third and fourth count values if said second count value reaches said words per fixed size portion of egress traffic parameter.

92. (previously presented) The apparatus of claim 91 wherein said counting with a third count value is timed with a first clock that times the removal of words from said egress FIFO buffer and wherein said counting with a fourth count value is timed with a second clock that times the storing of words into said egress FIFO buffer.

93. (previously presented) The apparatus of claim 84 further comprising means for counting, with a first count value, the number of words that have been stored into said ingress FIFO buffer.

94. (previously presented) The apparatus of claim 93 further comprising means for resetting said first count value to a first reset value if said first count value reaches said words per fixed size portion of ingress traffic parameter.

95. (previously presented) The apparatus of claim 93 further comprising means for counting, with a second count value, the number of words that have been removed from said ingress FIFO buffer.

96. (previously presented) The apparatus of claim 95 further comprising means for resetting said second count value to a second reset value if said second count value reaches said words per fixed size portion of ingress traffic parameter.

97. (previously presented) The apparatus of claim 95 further comprising means for counting with a third count value and counting with a fourth count value, said means for counting with a third and fourth count values further comprising:

1) means for incrementing said third and fourth count values if said first count value reaches said words per fixed size portion of ingress traffic parameter; and,

2) means for decrementing said third and fourth count values if said second count values reaches said words per fixed size portion of ingress traffic parameter.

98. (previously presented) The apparatus of claim 97 wherein said counting with a third count value is timed with a first clock that times the storing of words into said ingress FIFO buffer and wherein said counting with a fourth count value is timed with a second clock that times the removal of words from said ingress FIFO buffer.

99. (previously presented) A method, comprising:
programming a bits per word size parameter for an egress first-in-first-out (FIFO) buffer and programming a words per fixed size portion of egress traffic parameter for said egress FIFO buffer;

programming a bits per word size parameter for an ingress first-in-first-out (FIFO) buffer and programming a words per fixed size portion of ingress traffic parameter for said ingress FIFO buffer;

receiving at said egress FIFO buffer fixed size portions of egress traffic sent from a switch;

identifying a boundary of a fixed size portion of egress traffic within said egress FIFO buffer based upon said programmed bits per word size parameter for said egress FIFO and said words per fixed size portion of egress traffic parameter;

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sending fixed size portions of ingress traffic from said ingress FIFO buffer to said switch; and

identifying a boundary of a fixed size portion of ingress traffic within said ingress FIFO buffer based upon said programmed bits per word size parameter for said ingress FIFO and said programmed words per fixed size portion of ingress traffic parameter.
